i960® MC/MX CPU Computers Using Silicon Substrate MCMs

- 10-38 MIPs Microminiaturized Computers With Processor, Memory and I/O in Pin-Compatible Multichip Modules
- Two MCM Options Provide Low-Power i960® MC Processor (MCP-96) or High-Speed JIAWG i960 MX Processor (MXP-96)
- 1.5 to 4 Mbytes Zero Wait State SRAM
- 512 Kbytes to 2 Mbytes Local Flash Memory
- Three 16-Bit Programmable Timers
- RS-232 Console Port
- Demultiplexed Local Bus With DMA
- Reprogrammable FPGAs With JTAG
- All Surface Mount MCM Package of Size 2" x 3" With 182 Leads on 50 Mil Centers
- MXP-96 Unique Features: 33rd Trusted Security Bit; Private/Unified Cache With Built-In Coherency; Variable 1x, 2x nL Bus Timing
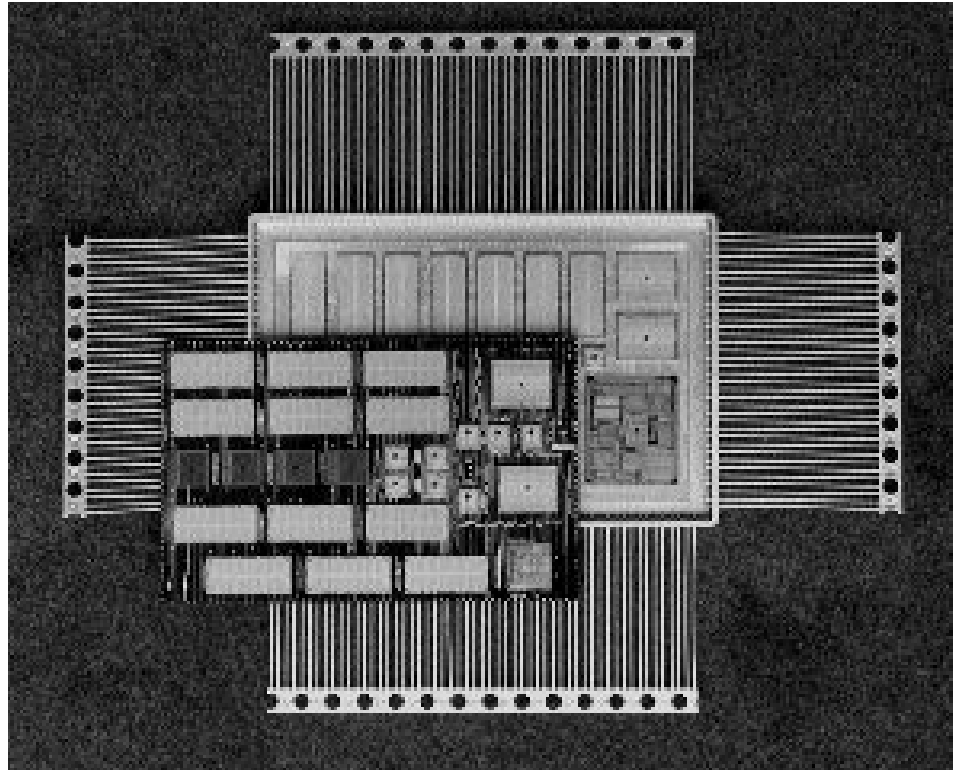
The MCP-96 and MXP-96 are a physically compatible pair of high density silicon MCMs that embed the i960 MC processor and JIAWG i960 MX microprocessors, respectively. Featuring a gull wing, 182-pin militarized package of only 2 inches by 3 inches, these miniature computers are organized to provide maximum simplicity and reliability to the user. All tactical interface signals, pin locations and timings are identical so that physical migration from the i960 MC processor version to the i960 MX processor version is achievable with no changes required in the target printed circuit board assembly.

The full 10 to 38 MIPs range of the i960 MC/MX microprocessor family is offered by this dual implementation, with all JIAWG requirements included in the MXP-96. All memory and input/output needed to achieve 33rd bit object-oriented address enforcement and data security are incorporated within this MCM.

The MXP-96 also provides 1 Mbyte

variable private and/or unified cache including MESI coherency control. Direct memory access is provided in both the MCP-96 and MXP-96 by allocating .5 Mbyte of the total 1.5 Mbyte SRAM to the local bus. In all cases the local bus is demultiplexed at the interface.

The unusually high density of these small MCMs is realized through the use of automatically produced silicon chip technology designed to eliminate the need for surface mounted decoupling capacitors. A full substrate decoupling capacitance is uniquely introduced between two solid power and ground planes within the silicon.

AVAILABILITY:
MCP-96 Now
MXP-96 Now

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